PATENT

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

Applicant:	FOO ET AL.	)	Examiner V. Kovalick
Appl. No.	10/647,723	)	Art Unit 2629
Confirm. No.	2166	)	Atty. Docket No. CS22497RA
Filed:	25 August 2003	)	

Title: "Matrix Display Having Addressable Display Elements And Methods"

RESPONSE UNDER 37 C.F.R. § 1.111

Assistant Commissioner for Patents
Alexandria, Virginia 22313

Sir:

Kindly amend the claims as indicated below.

In The Claims:

1. (Original) A method of activating a display element of a display device having n x m array of display elements, each display element coupled to a logic controlled switch, the method comprising:

applying a row address input and a row electrode input to control logic of the logic controlled switch of the display element;

applying a column address input and a column electrode input to the control logic of the logic controlled switch of the display element;

activating the display element with the logic controlled switch when the row address and row electrode inputs and when the column address and column electrode inputs satisfy a condition.

2. (Currently Amended) The method of Claim 1,

comparing the row address input and the row electrode input,

comparing the column address input and the column electrode input,

activating the display [~~pixel~~] element with the logic controlled switch based on results of the comparisons.

3. (Original) The method of Claim 2, controlling the logic-controlled switch includes enabling and disabling the logic controlled switch with a charging capacitor.

4. (Original) The method of Claim 1,

activating at least some display elements of the display device at a first refresh rate,

activating other display elements of the display device at a second refresh rate, different than the first refresh rate.

5. (Currently Amended) A method in a display device comprising an n x m array of addressable display elements, the method comprising:

activating at least some display elements characterizing a foreground image at a first rate;

activating other display elements characterizing a background image at a second rate,

the second [~~refresh~~] rate less than the first [~~refresh~~] rate;

activating the display elements with a corresponding logic controlled display element switch when row address and row electrode inputs and when the column address and column electrode inputs satisfy a condition.

Claim 6 (Cancelled).

7. (Currently Amended) The method of Claim 6,

comparing the row address input and the row electrode input,

comparing the column address input and the column electrode input,

activating the display element with the logic controlled display element switch using the results of the comparisons.

8. (Currently Amended) The method of Claim 7, enabling and disabling the logic controlled display element switch with a switch enabling charging capacitor [~~gate~~] controlled by the results of the comparisons.

9. (Original) The method of Claim 5, activating other display elements at the second rate includes not activating the other display elements.

10. (Original) A display device comprising:

a plurality of display elements arranged in a matrix,

each display element including a display pixel coupled to a switch,

each display element including an addressable latch having an output coupled to a controlling input of the switch,

the addressable latch having a row address input and a column address input.

11. (Original) The device of Claim 10, the addressable latch having a row electrode input and a column electrode input.

12. (Original) The device of Claim 10,

the addressable latch of each display element including row address logic and column address logic having corresponding outputs coupled to the output of the addressable latch,

the row address input coupled to the row address logic, the column address input coupled to the column address logic.

13. (Original) The device of Claim 10,

the addressable latch of each display element including first and second comparators, the first comparator having the row address input and a

row electrode input, the second comparator having the column address input and a column electrode input,

each display element including a logic device having a first input coupled to an output of the corresponding first comparator, the logic device having a second input coupled to an output of the corresponding second comparator.

14. (Original) The device of Claim 13, the logic device is an AND gate, the output of the addressable latch is an output the logic device

15. (Original) The device of Claim 13, a pixel capacitor connected parallel with the display pixel, and a switch enabling capacitor coupled to an input of the switch.

16. (Original) The device of Claim 10 is a thin-film-transistor display device.

17. (Currently Amended) A method in a display device comprising an n x m array of addressable display elements, the method comprising:

selectively activating display elements by individually addressing the display elements to be activated, <u>activating the display elements includes,</u>

<u>applying a row address input and a row electrode input to control logic of the corresponding display element,</u>

<u>applying a column address input and a column electrode input to the control logic of the corresponding display element, and</u>

activating the display element with a logic controlled switch when the control logic inputs satisfy a condition;

reducing power consumption by addressing at least some of the display elements at a first frequency and addressing other display elements at a second frequency, the second frequency less than the first frequency.

Claim 18 (Canceled).

19. (Currently Amended) The method of Claim 17 [~~18~~],

comparing the row address input and the row electrode input with the control logic,

comparing the column address input and the column electrode input with the control logic,

activating the display element by enabling the logic controlled switch using the results of the comparisons.

20. (Original) The method of Claim 19, enabling and disabling the logic controlled switch with a switch enabling capacitor controlled by the control logic.

REMARKS

Request for Reconsideration, Informal Matters, Claims Pending

The non-final Office action mailed on 2 June 2006 has been considered carefully. Reconsideration of the claimed invention in view of any amendments above and the discussion below is respectfully requested.

Claims 1-5, 7-17 and 19-20 are pending.

Allowability of Claims Over Yasukawa, Kaplinski & Peacock

Rejection Summary

Claims 1-2, 10 and 11 stand rejected under 35 USC 103(a) as being unpatentable over by U.S. Publication No. 2003/0210363 (Yasukawa) taken with EP 0472594 (Kaplinsky) in view of U.S. Patent No. 3,609,703 (Peacock).

Allowability of Claim 1

Regarding Claim 1, the prior art fails to disclose or suggest a

> … method of activating a display element of a display device having n x m array of display elements, each display element coupled to a logic controlled switch, the method comprising:
>
> applying a row address input and a row electrode input to control logic of the logic controlled switch of the display element;
>
> applying a column address input and a column electrode input to the control logic of the logic controlled switch of the display element;

> activating the display element with the logic controlled switch when the row address and row electrode inputs and when the column address and column electrode inputs satisfy a condition.

The Examiner concedes that Yasukawa fails to disclose an addressable latch having row and column inputs associated with each display element, but asserts that Kaplinsky and Peacock meets this deficiency.

Contrary to the Examiner's assertion, there is no motivation or suggestion to combine Yasukawa, Kaplinsky and Peacock as suggested by the Examiner. Yasukawa is concerned with reducing flickering and degradation of image quality caused by stray light in TFT switched displays. Kaplinsky discloses a programmable logic device (PLD) that receives a data input and a control signal input. It is unlikely that one skilled in the art would drive the display elements of Yasukawa with the programmable logical device of Kaplinksy. Moreover, the Examiner admits that the combination of Yasukawa and Kaplinsky alone does not meet the limitations of Claim 1. Peacock however does not remedy the deficiencies of Yasukawa and/or Kaplinksy. Peacock discloses a matrix of comparison circuits for searching entries in a database. In Peacock, each comparison circuit resets a latch when row and column bits do not match. One skilled in the art would not look to the comparison circuit of Peacock to drive the display elements in Yasukawa. Claim 1 is thus patentably distinguished over the art.

Allowability of Claim 2

Claim 2 was amended for consistency with Claim 1. The prior art fails to disclose or suggest in combination with Claim 1

> …comparing the row address input and the row electrode input,
> comparing the column address input and the column electrode input,
> activating the display element with the logic controlled switch based on results of the comparisons

Contrary to the Examiner assertion, Peacock does not disclose or suggest activating a display element with a comparison circuit. The comparison circuits of Peacock do not compare row address and electrode inputs and/or compare column address and electrode inputs. In Peacock, the comparison circuit compares row and column data. Claim 2 is thus further patentably distinguished over the art.

Allowability of Claim 10

Regarding Claim 10, the prior art fails to disclose or suggest a

> … display device comprising:
> a plurality of display elements arranged in a matrix,
> each display element including a display pixel coupled to a switch,
> each display element including an addressable latch having an output coupled to a controlling input of the switch,
> the addressable latch having a row address input and a column address input.

Contrary to the Examiner's assertion, there is no motivation or suggestion to combine Yasukawa, Kaplinsky and Peacock as suggested by the Examiner. Yasukawa is concerned with reducing flickering and degradation of image quality caused by stray light in TFT switched displays. Kaplinsky discloses a programmable logic device (PLD) that receives a data input and a

control signal input. It is unlikely that one skilled in the art would drive the display elements of Yasukawa with the programmable logical device of Kaplinksy. Peacock does not remedy the deficiencies of Yasukawa and Kaplinsky. Peacock discloses a matrix of comparison circuits for searching entries in a database. In Peacock, each comparison circuit resets a latch when row and column bits do not match. One skilled in the art would not look to the comparison circuit of Peacock to drive the display elements in Yasukawa. Claim 10 is thus patentably distinguished over the art.

Allowability of Claim 11

Regarding Claim 11, the prior art fails to disclose or suggest in combination with Claim 10 "… the addressable latch having a row electrode input and a column electrode input."

Contrary to the Examiner assertion, Peacock does not disclose or suggest activating a display element with a comparison circuit. The comparison circuits of Peacock do not compare row address and electrode inputs and/or compare column address and electrode inputs. In Peacock, the comparison circuit compares row and column data. Claim 11 is thus further patentably distinguished over the art.

Allowability of Claims Over Yasukawa, Kaplinsky, Peacock & Santoro

Rejection Summary

Claims 1-2, 10 and 11 stand rejected under 35 USC 103(a) as being unpatentable over by U.S. Publication No. 2003/0210363 (Yasukawa) taken with EP 0472594 (Kaplinsky) in view of U.S. Patent No. 3,609,703 (Peacock) and U.S. Publication No. 2003/0020671 (Santoro).

Allowability of Claim 4

Regarding Claim 4, the prior art fails to disclose or suggest in combination with Claim 1

> … activating at least some display elements of the display device at a first refresh rate,
> activating other display elements of the display device at a econd refresh rate, different than the first refresh rate.

Santoro fails to meet the deficiencies of Yasukawa, Kaplinsky and Peacock in connection with the rejection of Claim 1, from which Claim 4 depends.

Allowability of Claim 5

Claim 5 was amended to include the limitations of Claim 6. Contrary to the Examiner's assertion, the prior art fails to disclose or suggest a

> … method in a display device comprising an n x m array of addressable display elements, the method comprising:
> activating at least some display elements characterizing a foreground image at a first rate;
> activating other display elements characterizing a background image at a second rate,
> the second rate less than the first rate;

> activating the display elements with a corresponding logic controlled display element switch when row address and row electrode inputs and when the column address and column electrode inputs satisfy a condition.

Yasukawa, Kaplinsky, Peacock and Santoro fail to disclose or suggest "... activating the display elements with a corresponding logic controlled display element switch when row address and row electrode inputs and when the column address and column electrode inputs satisfy a condition" as recited in Claim 5. Yasukawa is concerned with reducing flickering and degradation of image quality caused by stray light in TFT switched displays. Kaplinsky discloses a programmable logic device (PLD) that receives a data input and a control signal input. Peacock discloses a matrix of comparison circuits for searching entries in a database wherein each comparison circuit resets a latch when row and column bits do not match. One skilled in the art would not look to the comparison circuit of Peacock to drive the display elements in Yasukawa. Santoro is relied upon for teaching different refresh rates. Amended Claim 5 is thus patentably distinguished over the art.

Allowability of Claims Over Yasukawa, Santoro & Whitby

Rejection Summary

Claims 17-18 stand rejected under 35 USC 103(a) as being unpatentable over by U.S. Publication No. 2003/0210363 (Yasukawa) taken with U.S. Publication No. 2003/0020671 (Santoro) in view of EP 0608056 (Whitby).

Allowability of Claim 17

Claim 17 has been amended to include the limitations of Claim 18. The prior art fails to disclose or suggest in combination with Claim 1,

> … method in a display device comprising an n x m array of addressable display elements, the method comprising:
>
> selectively activating display elements by individually addressing the display elements to be activated, activating the display elements includes,
>
> applying a row address input and a row electrode input to control logic of the corresponding display element,
>
> applying a column address input and a column electrode input to the control logic of the corresponding display element, and
>
> activating the display element with a logic controlled switch when the control logic inputs satisfy a condition;
>
> reducing power consumption by addressing at least some of the display elements at a first frequency and addressing other display elements at a second frequency, the second frequency less than the first frequency.

Yasukawa is concerned with reducing flickering and degradation of image quality caused by stray light in TFT switched displays. Yasukawa does not disclose or suggest "… applying a row address input and a row electrode input to control logic of the corresponding display element, applying a column address input and a column electrode input to the control logic of the corresponding display element, and activating the display element with a logic controlled switch when the control logic inputs satisfy a condition…" as in Claim 17. Yasukawa does not disclose display elements having corresponding control logic with row/column address/electrode inputs. Santoro is relied upon for teaching different refresh rates and Whitby is relied upon for teaching a first refresh frequency less than a second refresh frequency. Amended Claim 17 is thus patentably distinguished over the art.

Prayer For Relief

In view of any amendments and the discussion above, the Claims of the present application are in condition for allowance. Kindly withdraw any rejections and objections and allow this application to issue as a United States Patent without further delay.

Respectfully submitted,

/ R K Bowler/

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